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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,302	10/21/2003	Brian Amick	03226.328001;SUN030060	6902

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,302	AMICK ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Original claims 1-20 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4-8 and 10-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller, Jr. et al., U.S. Patent No. 6,316,976 ("Miller").

As per claim 1, Miller teaches a computer system, comprising:

a delay array arranged to generate an output signal that is delayed with respect to an input signal by an amount indicated by a delay code provided to the delay array (fig. 3, delay line 13 generates CLCK OUT with respect to CLCK IN);

a shift controller operatively connected to the delay array and arranged to update the delay code dependent on a phase comparison of the input signal and the output signal (fig. 3, comprising phase detect 15); and

a detection circuit arranged to monitor the delay code, wherein, the detection circuit, in response to a predetermined condition of the delay code, causes a self-reset of the delay code to a value different than that of a value of the delay code at one of a previous reset and an initial startup of the delay array (fig. 3, reset mechanism 16; col. 6, lines 41-65).

As per claim 4, Miller teaches a shift register arranged to store the delay code and operatively connected to the shift controller (fig. 3, shift register 12).

As per claim 5, Miller teaches a value of the self-reset delay code indicates more delay being needed than a value of the delay code at one of the reset and the startup of the delay array (col. 6, lines 41-65).

As per claim 6, Miller teaches a value of the self-reset delay code indicates less delay being needed than a value of the delay code at one of the reset and the startup of the delay array (col. 6, lines 41-65).

As per claim 7, Miller teaches a strobe delay line arranged to delay a strobe signal by an amount of delay indicated by the delay code (fig. 1, delay line 101).

As per claim 8, Miller teaches a memory arranged to output the strobe signal to the strobe delay line (col. 7, lines 55-63).

As per claim 10, Miller teaches at least one of the delay array, the shift controller, and the detection circuit are digital (fig. 5).

As per claim 11, Miller teaches a computer system, comprising:

means for delaying an input signal to generate an output signal, the means for delaying being dependent on a delay code indicative of an amount of delay by which to delay the input signal (fig. 3, delay line 13);

means for comparing phases of the input signal and the output signal (phase detect 15);

means for updating the delay code dependent on the means for comparing phases (col. 5, lines 27-37);

means for monitoring the delay code (reset mechanism 16); and

means for resetting the delay code in response to a detected predetermined condition of the delay code, wherein the delay code is reset to a value different than a value of the delay code present at one of a previous reset and an initial startup of the means for delaying (col. 6, lines 41-65).

As per claim 12, Miller teaches means for storing the delay code (fig. 3, shift register 12).

As per claim 13, Miller teaches the means for resetting is configured to reset the delay code to a value indicative of more delay being needed than as indicated by a value of the delay code present at one of the previous reset and the initial startup (col. 6, lines 41-65).

As per claim 14, Miller teaches the means for resetting is configured to reset the delay code to a value indicative of less delay being needed than as indicated by a value of the delay code present at one of the previous reset and the initial startup (col. 6, lines 41-65).

As per claim 15, Miller teaches means for delaying an incoming signal from an external memory dependent on the delay code (fig. 1, delay line 101).

As per claim 16, Miller teaches a method for performing delay locked loop operations, comprising:

delaying an input signal to generate an output signal, wherein the output signal is delayed with respect to the input signal by an amount indicated by a delay code (fig. 3, with delay line 13);

comparing phases of the input signal and the output signal (with phase detect 15);

updating the delay code dependent on the comparing (col. 5, lines 27-37); and

monitoring the delay code for a predetermined condition (with reset mechanism 16), wherein, in response to detecting the predetermined condition, resetting the delay code to a value different than a value of the delay code present at least at one of a previous reset and an initial startup of the delaying (col. 6, lines 41-65).

As per claims 17-20, since Miller teaches the system of claims 11-15 and the method of claim 16, Miller teaches the claimed method.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller, Jr. et al., U.S. Patent No. 6,316,976 ("Miller"), as applied to claim 1 above.

As per claim 3, Miller teaches the shift controller may comprises a phase comparator that may be configured in alternative ways (col. 5, lines 4-20), but does not expressly teach the phase comparator comprises a D flip-flop. Implementing phase comparators with a D flip-flop is well known in the art. Thus at the time of the invention, it would have been obvious to one of ordinary skill in the art that the phase comparator may comprise a D flip-flop.

As per claim 2, it would have been a matter of design to consider the detection circuit as part of the shift controller.

As per claim 9, clocking a data buffer with a strobe is well known in synchronous data transfer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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